REMARKS/ARGUMENTS

Introductory Comments

Reconsideration of this application is respectfully requested. Claims 31-57 are currently pending and stand rejected in the application.

Any reference to the "Office Action" refers to the Final Office action dated May 19, 2005. Any reference to the "Advisory Action" refers to the Advisory Action dated October 5, 2005.

Rejections Under 35 U.S.C. § 102(e)

In the office action dated May 19, 2004, claims 31-45, and 47-55 stand rejected under 35 U.S.C. §102(e) as anticipated by US 6,555,208 of Takada, et al. (hereinafter Takada). The office action asserts "Takada discloses, referring to figure 4, a printed circuit board (PCB) comprising:...at least one padless via (203) extending from the first signal routing layer to the electrically conductive layer, the at least one padless via in electrical contact with the electrically conductive layer (see col. 14, lines 10-20) ", (Office action, page 2, paragraph 4.) The office action further asserts applicants' arguments that Takada fails to teach a padless via are not persuasive because Takada's statement regarding "*the above conductor pattern* is all conductive patterns which are able to be formed on the surface of the insulating substrate such as a wiring circuit . . .etc.", teaches a padless via on the grounds that a wiring circuit is "fundamentally different from [a] pad", (Office action, page 8, paragraph 1) (emphasis provided). Applicants respectfully submit the office action, and subsequently the advisory action, misconstrues the cited recitation in Takada, and that when read in context, the recitation

does fully and conclusively supporting applicants' arguments as would be 'readily understood to the ordinarily skilled artisan'.

The portion cited by the office action is found in Takada's description of "[a] third invention", (column 6, line 66 – column 7, line 2). Takada explicitly establishes the proper context of 'the above conductor pattern' as separate from and co-existing with a 'pad';

> "*a pad* for external connection arranged *in an outermost layer of the insulating substrate*, a *conductor pattern arranged in another layer different from said outermost layer*, and a hole for conductivity *for electrically connecting said pad for external connection and said conductor pattern*", (column 6, lines 21-26) (emphasis provided).

Thus, Takada discloses three separate structures co-existing in the 'third invention'; a pad, a conductor pattern, and a hole.

Herein, Takada discloses that the 'conductor pattern' cited by the office action is 'in another layer different from said outermost layer', the aforementioned outermost layer being the one containing the 'pad' described by Takada; "a pad for external connection arranged in an outermost layer of the insulating substrate". By this disclosure, Takada explicitly discloses that not only are the 'pad' and the 'conductor pattern' separate and co-existing structures of the third invention, but they are also located in separate layers of the insulating substrate.

Lastly, Takada discloses, "[t]he pad for external connection is arranged *so as to form the bottom portion of the hole* for conductivity. Therefore, it is not necessary to form a conductor pattern for connecting the hole for conductivity and the pad for external connection", (column 6, lines 35-39)(emphasis provided). Here, Takada discloses that the pad 'is arranged so as to form the bottom portion of the hole', demonstrating

conclusively that the hole and the pad are integrated, thus disclosing a via with a pad, not a 'padless' via as claimed by applicants.

Therefore, although Takada discloses that the 'conductor pattern' recited in the office action may comprise "a wiring circuit...etc.", applicants have conclusively shown that the referenced 'conductor pattern' is a separate structure from the 'pad', so Takada's recited alternative embodiments for the 'conductor pattern' do not apply to or alter the presence of the 'pad' disclosed by Takada as "form[ing] the bottom portion of the hole"; a via which is not 'padless'.

Likewise, as previously demonstrated by applicants in the response filed 24 January 24, 2005 and the 'after final' response filed June 13, 2005, only vias with pads, and not padless vias, are disclosed throughout Takada. This is not a 'limited reading' of Takada by applicants, but rather the explicit teaching of Takada when taken as a whole. However, for clarity, applicants provide below a detailed demonstration of each instance supporting this assertion.

Takada Embodiment Mode Example 1 ('Embodiment 1')

No via is disclosed in Embodiment 1, (column 12, line 58 – column 14, line 5). Therefore, Embodiment 1 does not disclose applicants' recited claims.

Takada Embodiment Mode Example 2 ('Embodiment 2')

Referring to FIG. 4, Takada clearly recites and shows what is ordinarily and customarily referred to by those skilled in the art as a pad. "An upper end portion **231** of the hole **203** for conductivity is surrounded by the upper face pattern **201** having 0.025 mm in width B", (column 14, lines 24-26). The referenced 'width B' is in FIG. 5, clearly showing a pad **201** of upper face pattern surrounding the hole (via) **203**. Interpreting

Takada's upper face pattern 201, clearly shown in FIG. 4, as anything other than a pad requires assigning an interpretation of the figure and structure contrary to that of ordinary and customary usage in the art. Therefore, the via **203**, as taught by Takada, has a pad **201**, and therefore cannot be reasonably construed as being padless.

Takada Embodiment Mode Example 3 ('Embodiment 3')

Embodiment 3 (column 15, lines 40-58), is defined in Takada as "an embodiment mode example of the second invention", similar in the pertinent facts to those in Embodiment 2. No disclosures are provided altering or contradicting the presence of a via **203** with a pad **201** as presented in Embodiment 2. Therefore, Embodiment 3 cannot be reasonably construed as disclosing a padless via.

Takada Embodiment Mode Example 4 ('Embodiment 4')

Referring to FIG. 8, Takada clearly recites and shows,

> "the printed wiring board **341** in this example has...*a pad* **301** for external connection arranged in an outermost layer of the insulating substrate **305**, *conductor patterns* **325, 326** arranged in another layer different from the outermost layer, *and holes* **331, 332** *for conductivity, electrically connecting the pad* **301** *for external connection and the conductor patterns* **325, 326**", (column 15, line 63 – column 16, line 3)(emphasis added).

This language closely coincides with the language identified above with respect to 'a third invention' of Takada.

> "A third invention is a printed wiring board having an insulating substrate constructed by one, two or more insulating layers, *a pad* for external connection arranged in an outermost layer of the insulating substrate, a *conductor pattern* arranged in another layer different from said outermost layer, *and a hole for conductivity for electrically connecting said pad for external connection and said conductor pattern*", (column 6, lines 19-26)(emphasis added).

Therefore, when Takada later recites "the above conductor pattern is all conductive patterns which are able to be formed on the surface of the insulating substrate

such as a wiring circuit, a pad, a terminal, a land, etc.", as cited by the examiner, it is evident that 'the conductive patterns' therein recited are the conductor patterns recited in column 6, lines 22-23 and 25-26, and shown in FIG. 8 and recited regarding Embodiment 3 as conductive patterns **325, 326** and not the pad **301.** Takada clearly distinguishes the pad **301** and the conductive patterns **325, 326** and clearly states that they co-exist within the 'printed wiring board'.

Therefore, as clearly set forth by Takada, although the conductive patterns may be "all conductive patterns which are able to be formed on the surface of the insulating substrate such as a wiring circuit, a pad, a terminal, a land, etc.", this does not alter or negate that the pad also recited by Takada is and remains a pad, and therefore, the via disclosed by Takada cannot reasonably be construed as being padless.

Takada Embodiment Mode Example 5 ('Embodiment 5')

Embodiment 5 (column 18, lines 54-67), is defined in Takada as "an embodiment mode example of the third invention", similar in the pertinent facts to those in Embodiment 5. No disclosures are provided altering or contradicting the presence of a via (holes **331, 332**) with a pad **301**, and separately and independently, conductor patterns **325, 326** as presented in Embodiment 4. Therefore, Embodiment 5 cannot be reasonably construed as disclosing a padless via.

Takada Embodiment Mode Example 6 ('Embodiment 6')

Takada states that Embodiment 6 discloses a fourth invention explained by FIGS. 18-27. With regard to the fourth invention, Takada states;

> The conductor pattern 401 is constructed by a land 411 of the through hole 405, a terminal 413 for joining a bond wire 461 connected to an electronic part 60, a wiring circuit 412 for electrically connecting the land 411 and the

terminal 413 to each other, *and a pad* **414** for joining a soldering ball 4", (column 19, lines 11-16) (emphasis provided).

Takada's FIG. 20 clearly shows a pad **414** adjoined with a via **405**. Therefore, the via **405**, as taught by Takada, cannot be reasonably construed as being padless.

Therefore, applicants respectfully submit that Takada fails to teach applicants' recitation of "at least one padless via", recited in each of applicants independent claims 31, 36, 41, 47, and 54, that the 35 U.S.C. 102(e) rejections applied to each and every independent claim have been fully traversed, and that examiner's assertions in the "Response to Arguments" have been fully rebutted. For at least these reasons, applicants request the rejections be withdrawn. Inasmuch as claims 32-35, 37-40, 42-44, 48-53, and 55 depend from and include the recitations of independent claims 31, 36, 41, 47, and 54, respectively, applicants submit the 35 U.S.C. §102(e) rejection of each of these claims is likewise improper and request the rejections be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

In the office action, claim 44 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Takada. The office action asserts that Takada discloses the claimed invention, except that Takada does not specifically state that a width of the at least two conductive traces is approximately 3 mils. Instead, Takada generically states that the width can be varied, (Takada, column 15, lines 25-35). Thus, the office action asserts that forming the claimed traces with a width of 3 mils would be obvious to one of ordinary skill in the art at the time of the invention, (office action, page 6, paragraph 2). Applicants respectfully disagree that this is so.

As applicants demonstrated in the prior section, Takada fails to disclose applicants' invention inasmuch as Takada fails to disclose the "at least one padless via" recited in applicants' independent claim 41, from which claim 44 depends. Therefore, applicants respectfully submit that the U.S.C. §103(a) rejection of claim 44 is improper and should be withdrawn.

The office action further rejects claims 46, 56, and 57 under 35 U.S.C. 103(a) as being unpatentable over Takada in light of US 2003/0001287 (hereinafter Sathe), (office action, page 6, paragraph 4). The office action asserts that Takada discloses the claimed invention, except Takada does not specifically state that the PCB is a motherboard and the component is a processor. However, the office action further asserts that the disclosure of Sathe demonstrates it is well known in the art that Takada's PCB could be considered a motherboard, and that processors are attached to said boards, (office action, page 7, paragraph 1) Additionally, the office action states that at the time of invention, it would have been obvious to comprise the component of a well known BGA package or LGA package, (office action, page 7, paragraph 2) Therefore, the office action asserts it would have been obvious to one having ordinary skill in the art, at the time of invention, to comprise the board and component in Takada of a motherboard and processor respectively.

As applicants demonstrated in discussion of the 35 U.S.C. 102(e) rejection, Takada fails to disclose applicants' invention inasmuch as Takada fails to disclose at least one padless via claimed in independent claims 41 and 54, from which claims 46, and 56 & 57 depend, respectively. As cited in the office action, the recitations of Sathe are

unrelated to padless vias, and so the combination of Takada with Sathe also fails to teach or make obvious applicants' invention including the at least one padless via.

Therefore, applicants respectfully submit that the U.S.C. §103(a) rejection of claim 46, 56 & 57 is improper and should be withdrawn. Takada fails to disclose the at least one padless via in applicants' independent claims, and the cited combination of Takada with Sathe fail to make obvious applicants' invention including the at least one padless via. Therefore, the combined references are improper as a basis for a 35 U.S.C. 103(a) rejection for claims 46, 56, and 57.

CONCLUSION

In light of the points and arguments set forth herein, applicants respectfully submit that the rejections have been properly overcome, and the claims are allowable as they stand.

Please charge any shortages and credit any overages to Deposit Account No. 02-2666.

Respectfully submitted,

Date: October 14, 2005

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